Amendments to the Claims

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

1. (Amended) A digital phased array receiver for receiving electromagnetic energy, comprising:
   a plurality of antenna elements capable of receiving electromagnetic energy; and
   a receive module coupled to each of the plurality of antenna elements, the receive module including an analog to digital converter controlled by a clock signal generated by clock circuitry coupled to a delay circuit;
   wherein each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled.

2. (Amended) The digital phased array receiver of claim 1, wherein each analog to digital converter has a multiple bit digital value as an output.

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3. (Amended) The digital phased array receiver of claim 1, wherein each analog to digital converter is a single bit digital value as an output.

4. (Amended) The digital phased array receiver of claim 1, further comprising multiple data conversion circuits coupled to receive the output of each analog to digital converter at a first clock rate and having an output signal at a second clock rate.

5. (Amended) The digital phased array receiver of claim 4, wherein the first clock rate matches the base clock signal and the second clock rate is slower than the first clock rate.

6. (Amended) The digital phased array receiver of claim 1, wherein an amount of delay provided by each delay circuit is programmable.

7. (Amended) The digital phased array receiver of claim 6, wherein the plurality of antenna elements are grouped into sets of antenna elements and wherein each antenna element within the same set has the same amount of programmed delay.

8. (Amended) The digital phased array receiver of claim 1, wherein the electromagnetic energy is radio-frequency energy.

9. (Original) A digital phased array receive-path module, comprising:

an analog to digital converter having an analog input signal representative of received electromagnetic energy;

clock circuitry having a clock output signal; and

time delay circuitry coupled to the clock output signal to provide a relative delay to the clock output signal, the delayed clock output signal being coupled to the analog to digital converter to control a sampling rate for the analog to digital converter.

10. (Original) The digital phased array receive-path module of claim 9, wherein the analog to digital converter has a multiple bit digital value as an output.

11. (Original) The digital phased array receive-path module of claim 9, wherein the analog to digital converter is a single bit digital value as an output.

12. (Original) The digital phased array receive-path module of claim 9, wherein an amount of delay provided by the delay circuit is programmable.

13. (Original) The digital phased array receive-path module of claim 12, wherein the delay circuit is controlled by a digital word provided by a control register that may be loaded with a desired delay value.

14. (Original) The digital phased array receive-path module of claim 9, further comprising synchronization circuitry coupled to the analog to digital converter to receive and then output data from the analog to digital converter at an output clock rate.

15. (Original) The digital phased array receive-path module of claim 14, wherein the output clock rate for the synchronization circuitry matches the clock signal controlling the analog to digital converter.

16. (Original) The digital phased array receive-path module of claim 9, wherein the electromagnetic energy is radio-frequency energy.

17. (Amended) A digital phased array transmitter for transmitting electromagnetic energy, comprising:

a plurality of antenna elements capable of transmitting electromagnetic energy; and

a transmit module coupled to each of the plurality of antenna elements, the transmit module including a digital to analog converter controlled by a clock signal generated by clock circuitry coupled to a delay circuit;

wherein each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled.

18. (Amended) The digital phased array transmitter of claim 17, wherein each digital to analog converter has a multiple bit digital value as an input.

19. (Amended) The digital phased array transmitter of claim 17, wherein each digital to analog converter is a single bit digital value as an input.

20. (Amended) The digital phased array transmitter of claim 17, further comprising multiple data conversion circuits coupled to provide an output signal to each analog to digital converter at a first clock rate and having an input signal at a second clock rate.

21. (Amended) The digital phased array transmitter of claim 20, wherein the first clock rate matches the base clock signal and the second clock rate is slower than the first clock rate.

22. (Amended) The digital phased array transmitter of claim 17, wherein an amount of delay provided by each delay circuit is programmable.

23. (Amended) The digital phased array transmitter of claim 22, wherein the plurality of antenna elements are grouped into sets of antenna elements and wherein each antenna element within the same set has the same amount of programmed delay.

24. (Amended) The digital phased array transmitter of claim 17, wherein the electromagnetic energy is radio-frequency energy.

25. (Original) A digital phased array transmit-path module, comprising:

a digital to analog converter having a digital input signal representative of electromagnetic energy to be transmitted;

clock circuitry having a clock output signal; and

programmable time delay circuitry coupled to the clock output signal to provide a relative delay to the clock output signal, the delayed clock output signal being coupled to the digital to analog converter to control a operational rate for the digital to analog converter.

26. (Original) The digital phased array transmit-path module of claim 25, wherein the digital to analog converter has a multiple bit digital value as an output.

27. (Original) The digital phased array transmit-path module of claim 25, wherein the digital to analog converter is a single bit digital value as an output.

28. (Original) The digital phased array transmit-path module of claim 25, wherein an amount of delay provided by the delay circuit is programmable.

29. (Original) The digital phased array transmit-path module of claim 28, wherein the delay circuit is controlled by a digital word provided by a control register that may be loaded with a desired delay value.

30. (Original) The digital phased array transmit-path module of claim 25, further comprising synchronization circuitry coupled to the digital to analog converter to receive and then output data to the digital to analog converter at an output clock rate.

31. (Original) The digital phased array transmit-path module of claim 30, wherein the output clock rate for the synchronization circuitry matches the clock signal controlling the digital to analog converter.

32. (Original) The digital phased array transmit-path module of claim 25, wherein the electromagnetic energy is radio-frequency energy.

33. (Amended) A digital phased array transceiver for receiving and transmitting electromagnetic energy, comprising:

a plurality of antenna elements capable of receiving and transmitting electromagnetic energy;

a receive module coupled to each of the plurality of antenna elements, each receive module including an analog to digital converter controlled by a clock signal generated by clock circuitry coupled to a programmable delay circuit, wherein each programmable delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled; and

a transmit module coupled to each of the plurality of antenna elements, each transmit module including a digital to analog converter controlled by a clock signal generated by clock circuitry coupled to a programmable delay circuit, wherein each programmable delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled.

34. (Amended) The digital phased array transceiver of claim 33, wherein the electromagnetic energy is radio frequency energy.

35. (Original) A digital phased array transmit/receive module, comprising:

an analog to digital converter having an analog input signal representative of received electromagnetic energy;

a digital to analog converter having a digital input signal representative of electromagnetic energy to be transmitted;

clock circuitry having a clock output signal; and

programmable time delay circuitry coupled to the clock output signal to provide a relative delay to the clock output signal, the delayed clock output signal being coupled to the analog to digital converter to control a sampling rate for the analog to digital converter and being coupled to the digital to analog converter to control a operational rate for the digital to analog converter.

36. (Original) The digital phased array of claim 35, wherein the electromagnetic energy is radio frequency energy.

37. (Original) The digital phased array of claim 35, wherein the programmable delay circuitry comprises a first time delay circuit having a clock output for the analog to digital converter and a second time delay circuit having a clock output for the digital to analog converter.

38. (Original) The digital phased array of claim 35, wherein the programmable delay circuitry comprises a single time delay circuit having a single clock output for both the analog to digital converter and the digital to analog converter.

39. (Original) The digital phased array of claim 35, wherein the programmable delay circuitry comprises digitally programmable micro-electromechanical switch (MEMS) phase shifters.

40. (Original) The digital phased array of claim 35, wherein the programmable delay circuitry comprises digitally programmable diode phase shifters.

41. (Original) The digital phased array of claim 35, wherein the programmable delay circuitry comprises digitally programmable field effect transistor (FET) switching devices.

42. (Original) A method for receiving electromagnetic energy, comprising:

receiving analog electromagnetic energy with a plurality of antenna elements;

converting analog information from the plurality of antenna elements to digital information utilizing an analog to digital converters associated with the antenna elements; and

controlling each analog to digital converter with a clock signal generated by clock circuitry coupled to a delay circuit so that each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a receive direction of the plurality of antenna elements may be electronically controlled.

43. (Original) The method of claim 42, wherein each analog to digital converter has a multiple bit digital value as an output.

44. (Original) The method of claim 42, wherein each analog to digital converter has a single bit digital value as an output.

45. (Original) The method of claim 42, wherein an amount of delay provided by each delay circuit is programmable.

46. (Original) The method of claim 45, further comprising grouping the plurality of antenna elements into sets of antenna elements and setting the same amount of programmed delay for each antenna element within the same set.

47. (Amended) The method of ~~claim 37~~ claim 42, wherein the electromagnetic energy is radio-frequency energy.

48. A method for processing received electromagnetic energy, comprising:
converting analog information representative of received electromagnetic energy to digital information utilizing an analog to digital converter;
generating a clock signal that includes a delay; and
controlling the sampling rate for the analog to digital converter with the clock signal.

49. (Original) The method of claim 48, wherein the analog to digital converter has a multiple bit digital value as an output.

50. (Original) The method of claim 48, wherein the analog to digital converter has a single bit digital value as an output.

51. (Original) The method of claim 48, further comprising programming the amount of delay included in the clock signal.

52. (Original) The method of claim 48, wherein the electromagnetic energy is radio-frequency energy.

53. (Original) A method for transmitting electromagnetic energy, comprising:
converting digital information to analog information utilizing a plurality of digital to analog converters associated with a plurality of antenna elements;
controlling each digital to analog converter with a clock signal generated by clock circuitry coupled to a delay circuit so that each delay circuit delays a base clock signal from the clock circuitry by a desired amount so that a transmit direction of the plurality of antenna elements may be electronically controlled; and
transmitting electromagnetic energy in the transmit direction.

54. (Original) The method of claim 53, wherein each digital to analog converter has a multiple bit digital value as an input.

55. (Original) The method of claim 53, wherein each digital to analog converter has a single bit digital value as an input.

56. (Original) The method of claim 53, wherein an amount of delay provided by each delay circuit is programmable.

57. (Original) The method of claim 56, further comprising grouping the plurality of antenna elements into sets of antenna elements and setting the same amount of programmed delay for each antenna element within the same set.

58. (Original) The method of claim 53, wherein the electromagnetic energy is radio-frequency energy.

59. (Original) A method for processing electromagnetic energy for transmission, comprising:

converting digital information representative of electromagnetic energy for transmission to analog information utilizing a digital to analog converter;

generating a clock signal that includes a delay; and

controlling the digital to analog converter with the clock signal.

60. (Original) The method of claim 59, wherein the digital to analog converter has a multiple bit digital value as an input.

61. (Original) The method of claim 59, wherein the digital to analog converter has a single bit digital value as an input.

62. (Original) The method of claim 59, further comprising programming the amount of delay included in the clock signal.

63. (Original) The method of claim 59, wherein the electromagnetic energy is radio-frequency energy.